Amendments to the Specification

Please replace the paragraph beginning on page 2, line 20 with the following amended paragraph:

There have also been proposed several methods such as a method for providing a conductive path between an SOI layer and an Si support substrate isolated by a BOX oxide film [[204]] in the SOI wafer to thereby control a substrate potential. A patent document 2 has proposed a method for forming a substrate contact in a buried oxide film that insulates an SOI layer and an Si support substrate from each other. A method for forming a short-circuit conductor for bringing an Si support substrate and an SOI layer into conduction in the neighborhood of a scribe-intended region has been proposed by a patent document 3. A patent document 4 has proposed a method for cutting a scribe line to thereby bring an Si support substrate and an SOI layer disposed above a buried oxide film.

Please replace the paragraph beginning on page 3, line 15 with the following amended paragraph:

Fig. 6 is a diagram schematically showing, by a sectional partly cut area, the manner in which electrical charges are stored by deposition of a metal layer by sputtering in a wiring process employed in a method for manufacturing a semiconductor device using an SOI wafer 200. In the drawing, the left end corresponds to a wafer edge 222. A semiconductor element is not formed in a wafer edge region 224

corresponding to a peripheral region extending to about 5mm in the direction (right direction here) of the center of the wafer as viewed from the wafer edge. A region near the wafer center from the wafer edge region 224 corresponds to a device forming region 226, where various devices are formed.

Please replace the paragraph beginning on page 3, line 25 with the following amended paragraph:

Here, the SOI wafer 200 comprises an Si support substrate 202, a BOX oxide film 204 and an SOI layer 206. The Si support substrate 202 and the SOI layer 206 are insulated from each other by the BOX oxide film 204 used as a buried oxide film. Individual devices formed in the SOI wafer 200 are separated from one another by device-to-device isolation regions 208. A detailed description thereof is omitted in Fig. 6, and a gate insulating film 210 and a gate electrode 212 are shown in Fig. 6. An interlayer insulating film 214 is deposited on the upper side of the SOI wafer 200 formed with the devices. A contact 216 for connecting to an upper wiring is formed over the gate electrode 212.

Please replace the abstract with the following amended abstract:

A resist pattern ~~(110a)~~ formed so as to expose a wafer edge region is used to expose an edge surface region [[(120)]] of an Si support substrate [[(102)]] by dry etching. Next, a conductive layer constituted as wirings by subsequent patterning is formed by sputtering.